

C1  
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flow rate ratio of said at least one fluorocarbon to said ammonia is from about 2:1 to about 40:1, and said flow rate of said ammonia is at least about 2 sccm.

C2  
2. (amended) The method of claim 1, wherein said method is performed to produce a self-aligned contact opening, said opening is self-aligned between two adjacent gate stack structures with side wall spacers.

6. (amended) The method of claim 4, wherein said etching is performed at an operating pressure of about 25 to about 60 milliTorr.

C3  
7. (amended) The method of claim 4, wherein said etching is performed at an operating pressure of about 40 to about 50 milliTorr.

C4  
8. (amended) The method of claim 1, wherein said etching is performed through a patterned photoresist mask.

C5  
13. (amended) The method of claim 2, wherein said side wall spacers remain unetched during formation of said self-aligned contact opening.

C6  
21. (amended) The method of claim 18, wherein said CF<sub>4</sub> is flowed into a reaction chamber at a flow rate of about 18 sccm.

C7

23. (amended) The method of claim 22, wherein said CHF<sub>3</sub> is flowed into a reaction chamber at a flow rate of about 40 sccm.

C8

25. (amended) The method of claim 24, wherein said CH<sub>2</sub>F<sub>2</sub> is introduced at a flow rate of about 13 sccm.

36. (three times amended) A process for forming an opening in an insulative layer formed over a substrate in a semiconductor device, said process comprising:

forming a pair of adjacent gate stacks in said insulative layer;

forming sidewall spacers on sidewalls of said adjacent gate stacks;

forming a patterned photoresist mask layer over said insulative layer; and,

etching an opening in said insulative layer defined at least in part by said sidewall spacers through an aperture in said patterned resist layer, wherein said opening is etched through to said substrate using a combination consisting essentially of ammonia and at least one fluorocarbon, wherein said fluorocarbon is selected from the group consisting of C<sub>4</sub>F<sub>8</sub>, C<sub>4</sub>F<sub>6</sub>, C<sub>5</sub>F<sub>8</sub>, CF<sub>4</sub>, C<sub>2</sub>F<sub>6</sub>, CHF<sub>3</sub>, CH<sub>2</sub>F<sub>2</sub> and C<sub>3</sub>F<sub>8</sub>, and wherein the flow rate ratio of said at least one fluorocarbon to said ammonia is from about 2:1 to about 40:1, and said flow rate of said ammonia is at least about 2 sccm.

C 10

37. (amended) The method of claim 36, wherein said etching is performed to produce a self-aligned contact opening in said insulative layer, said opening is self-aligned between said adjacent gate stack structures with sidewall spacers.

C 11

39. (amended) The process of claim 38, wherein said at least one fluorocarbon and said ammonia are flowed into said reaction chamber such the flow rate ratio of said fluorocarbon to said ammonia is not less than about 3:1.

C 12

41. (amended) The process of claim 36, wherein said flow rate ratio is within the range of about 4:1 to about 10:1.

C 13

64. (three times amended) A method of forming a conductive plug between adjacent gate stacks with sidewall spacers and inside a self-aligned contact opening formed in an insulative layer provided over a substrate in a semiconductor device, said method comprising:

contacting said insulative layer with a plasma etchant mixture consisting essentially of ammonia and at least one fluorocarbon at a temperature within the range of from about -50 to about 80 degrees Celsius so as to form a self-aligned contact opening defined at least in part by said sidewall spacers on adjacent gate stacks in said insulative layer without an etch stop, wherein said contacting further forms a protective layer over opposed sidewall spacers which have been formed over said adjacent gate stacks, wherein the flow rate ratio of said at least one fluorocarbon to said ammonia is from about 2:1 to about 40:1, and said flow rate of said ammonia is at least about 2 sccm; and,

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depositing a conductive plug inside said etched opening such that said conductive plug is separated from said sidewall spacers by said protective layer.